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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/018,783	02/04/1998	THOMAS L. RITZDORF	11928US01	1242
50689	7590	07/21/2006	EXAMINER	
PERKINS COIE LLP			NADAV, ORI	
P.O. BOX 1247			ART UNIT	
PATENT-SEA			PAPER NUMBER	
SEATTLE, WA 98111-1247			2811	

DATE MAILED: 07/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/018,783

Applicant(s)

RITZDORF ET AL.

Examiner

Ori Nadav

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 17 May 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,3,4,6,8-11,13-17,24-37 and 42-95 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3,4,6,8-11,13-17,24-37 and 42-95 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 8/19/02, 1/6/03.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

- The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 3, 4, 6, 8-11, 13-17, 24-37 and 42-95 are rejected under 35

U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitation of annealing process at a temperature below certain temperature, as recited in claims 1, 6, 10, 11, 24, 30, 51, 57, 70, 83, is held to be indefinite since applicant does not recite a lower limit to the temperature.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 3, 4, 6, 8-11, 13-17, 24-37 and 42-95, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ding et al. (6,066,892) in view of Venkatraman (5,677,244).

Regarding claim 10, Ding et al. teach in figure 3 and related text a method for filling recessed microstructures at a surface of a semiconductor work-piece, the work-piece

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including at least one low K dielectric layer 54, and a continuous copper seed layer 60 on the dielectric layer, the method comprising:

depositing copper 62 into contact with the seed layer 60 to form continuous copper in the recessed micro-structures using an electrochemical plating process that generates copper grains that are sufficiently small so as to substantially fill the recessed microstructures; and

subjecting the surface of the semiconductor work-piece with the deposited copper to an elevated temperature annealing process at a temperature selected to be below a predetermined temperature at which the dielectric layer would suffer substantial degradation.

Ding et al. do not teach a barrier layer on the dielectric layer.

Venkatraman teaches in figure 2 and related text a barrier layer 13 on the dielectric layer 15.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a barrier layer on the dielectric layer in Ding et al.'s device in order to prevent out diffusion of copper into the dielectric layer.

Regarding claims 11, 17, 29, 50 and 52, prior art teaches removing copper metallization from the surface of the work-piece except from the recessed microstructures after the annealing of the copper using CMP.

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Regarding claims 3-4, 8-9, 24, 30, 51, 53, 57, 70 and 83, Ding et al. teach depositing the copper layer using an electrolytic process.

Regarding claims 24, 35-36, 57, 70 and 83, Venkatraman teaches in figure 2 and related text subjecting the surface of the semiconductor work-piece with the deposited copper to an elevated temperature annealing process at a temperature below about 250 to 300 degrees Celsius for a time period that is sufficient to increase the grain size of the deposited copper (column 4, lines 13-14).

Regarding claims 1, 32, 37, 51, 58-59, 71-72 and 86-87, Ding et al. teach in figure 2 and related text substantially the entire claimed structure, as applied to claim 11 above, except subjecting the copper to a temperature annealing process at a temperature below about 100 degrees Celsius.

Venkatraman teaches in figure 2 and related text subjecting the surface of the semiconductor work-piece with the deposited copper to an elevated temperature annealing process at a temperature about 150 to 390 degrees, and that the anneal temperature can be varied to adjust the characteristics of the copper (column 4, lines 13-18).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to anneal the copper in Ding et al.'s device at a temperature below about 100 degrees Celsius, in order to adjust the characteristics of the copper according to the requirements of the application at hand.

Regarding claims 42, 44-46, 64-67, 70, 78-80, 83-85 and 93, Ding et al. teach in figure 3 and related text substantially the entire claimed structure, as applied to claim 11 above, except applying electroplating power to the seed layer as a first power level for a predetermined first period of time and then applying electroplating power to the seed layer a higher second power level, wherein the forward pulsed waveform is at a frequency of between 1 and 1000 Hz.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply electroplating power to the seed layer as a first power level for a predetermined first period of time and then apply electroplating power to the seed layer a higher second power level, wherein the forward pulsed waveform is at a frequency of between 1 and 1000 Hz, in Ding et al.'s device, in order to improve the characteristics of the copper layer.

Regarding claims 33, 51, 60-61, 73-74 and 88-89, Ding et al. teach in figure 3 and related text substantially the entire claimed structure, as applied to claim 11 above, except an annealing process for less than 15 minutes and less than one minute.

Venkatraman teaches in figure 2 and related text that the anneal time vary to adjust the characteristics of the copper (column 4, lines 13-18).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an annealing process for less than 15 minutes and less than one minute in Ding et al.'s device, in order to adjust the characteristics of the copper according to the requirements of the application at hand.

Regarding claims 13-16, 26-28, 55-56, 63, 76 and 91, prior art teaches applying a metal seed layer 30 over the barrier layer 13 using CVD and PVD.

### ***Response to Arguments***

Applicant argues that the claimed limitation of annealing process at a temperature below or equal to a certain temperature, as recited in claims 1, 6, 10, 11, 24, 30, 51, 57, 70, 83, is not indefinite, because the upper temperature has limits. The claimed limitation of annealing process at a temperature below certain temperature, as recited in claims 1, 6, 10, 11, 24, 30, 51, 57, 70, 83, is held to be indefinite since applicant does not recite a lower limit to the temperature. For example, a temperature of zero degrees can read on the claims, and clearly, a temperature of zero degrees will not increase the grain size.

The rest of applicant's arguments with respect to claims 1, 3, 4, 6, 8-11, 13-17, 24-37 and 42-95 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.



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Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'ORI NADAV', is positioned above the printed name.

O.N.  
7/17/06

ORI NADAV  
PRIMARY EXAMINER  
TECHNOLOGY CENTER 2800